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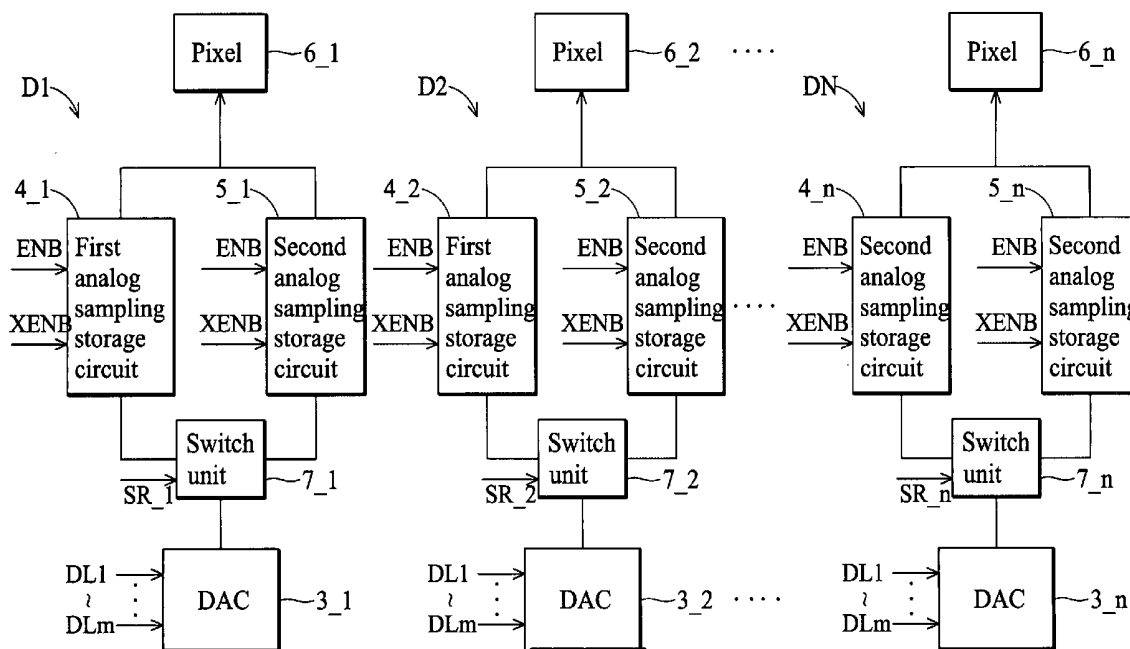
(19) **United States**(12) **Patent Application Publication** (10) **Pub. No.: US 2005/0270206 A1****Tseng et al.**(43) **Pub. Date:****Dec. 8, 2005**(54) **DATA DRIVING CIRCUIT FOR ORGANIC LIGHT EMITTING DIODE DISPLAY****Publication Classification**(51) **Int. Cl.⁷** **H03M 1/66**(52) **U.S. Cl.** **341/144**(75) Inventors: **Jung-Chun Tseng**, Neipu Township (TW); **Shin-Hung Yeh**, Taipei City (TW); **Wein-Town Sun**, Kaohsiung City (TW)(57) **ABSTRACT**

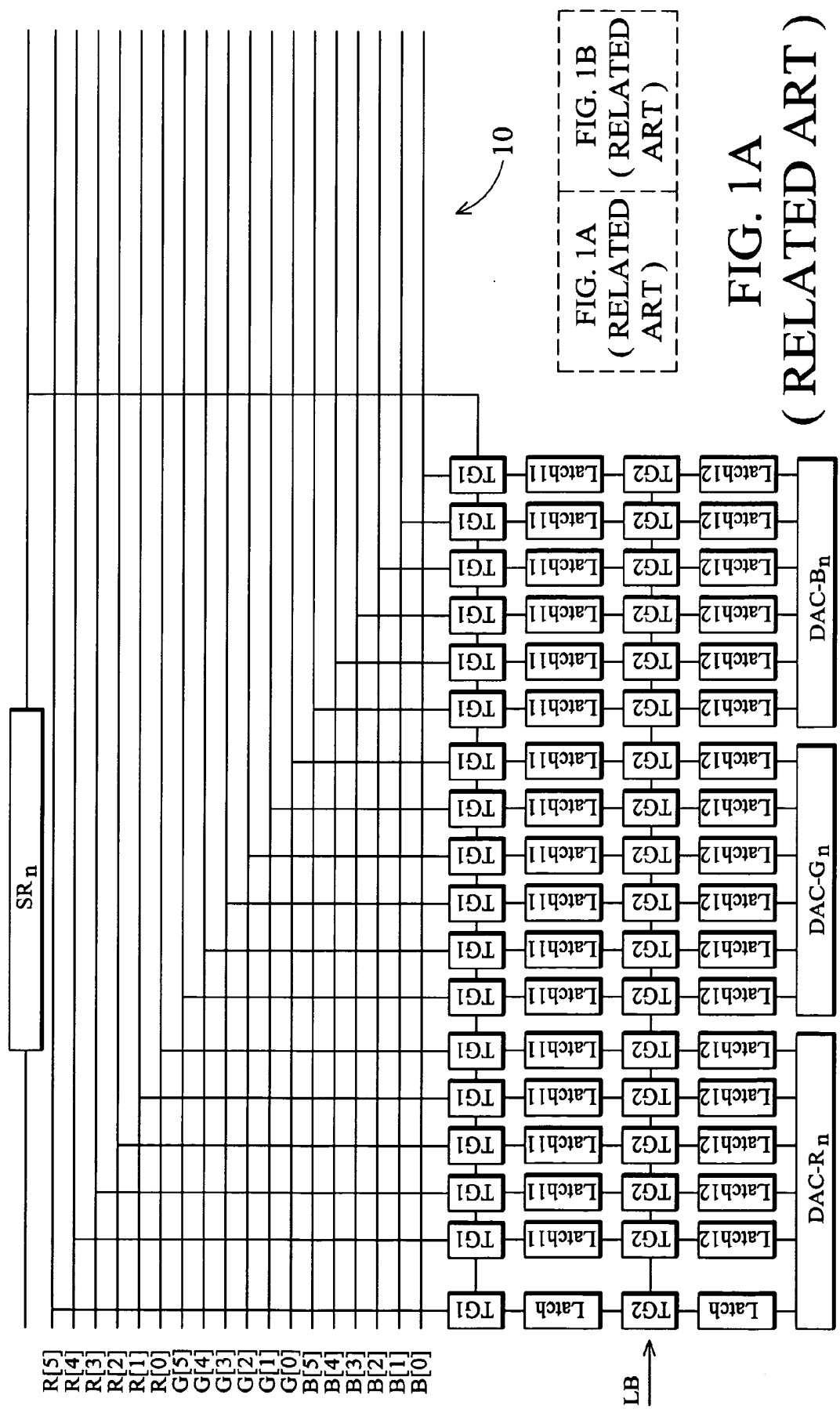
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A data driving circuit and organic light emitting diode display, comprising a D/A converter, a switch unit, a first analog sampling storage circuit and a second analog sampling storage circuit. The first analog sampling storage circuit is controlled by a first signal for storing corresponding first analog transformed data in the first cycle, and controlled by a second signal for outputting first analog data corresponding to the first analog transformed data in the second cycle. The second analog sampling storage circuit is controlled by the second signal for storing the second analog transformed data in the second cycle, and controlled by the first signal for outputting second analog data corresponding to the second analog transformed data in a third cycle.





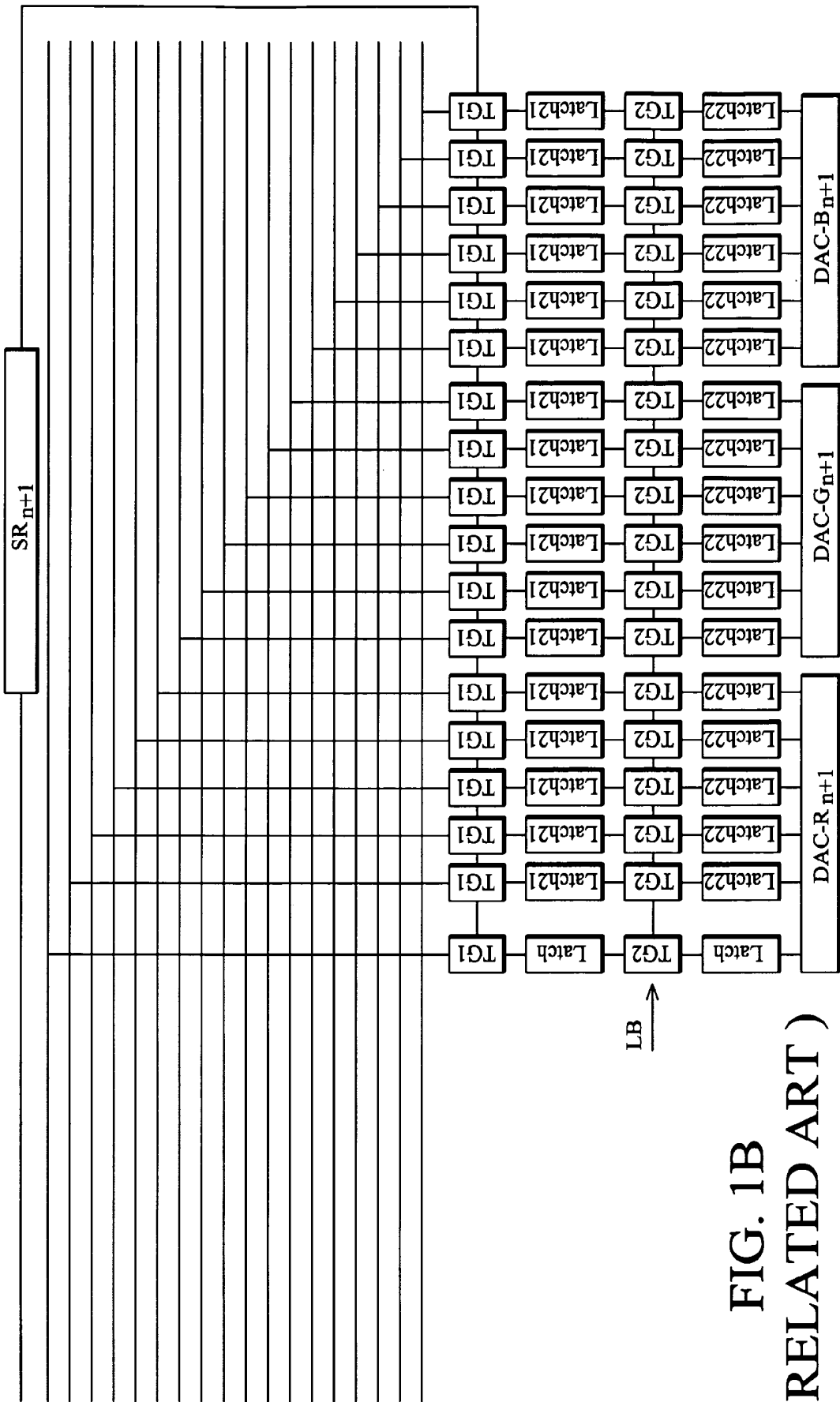


FIG. 1B
(RELATED ART)

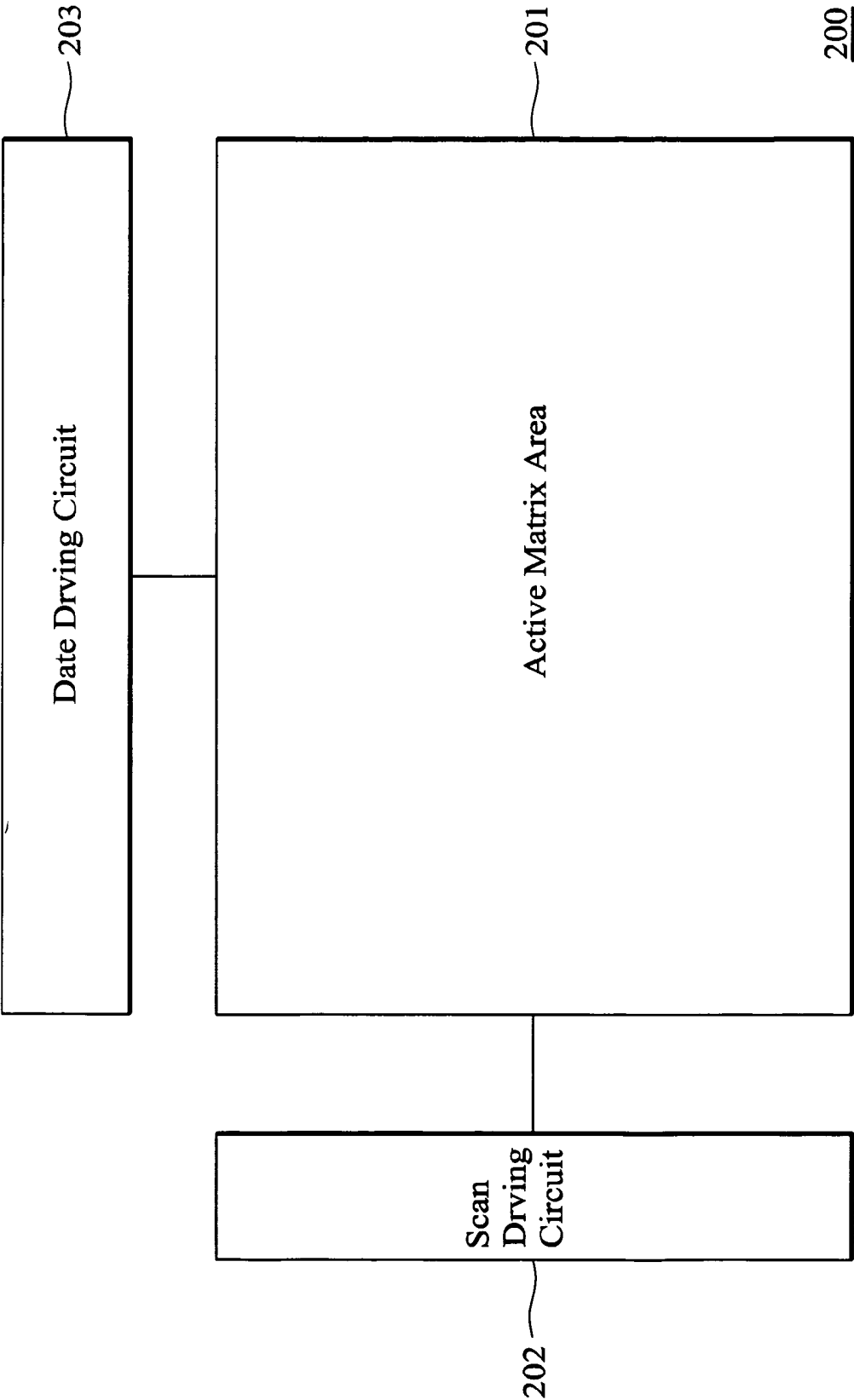


FIG. 2

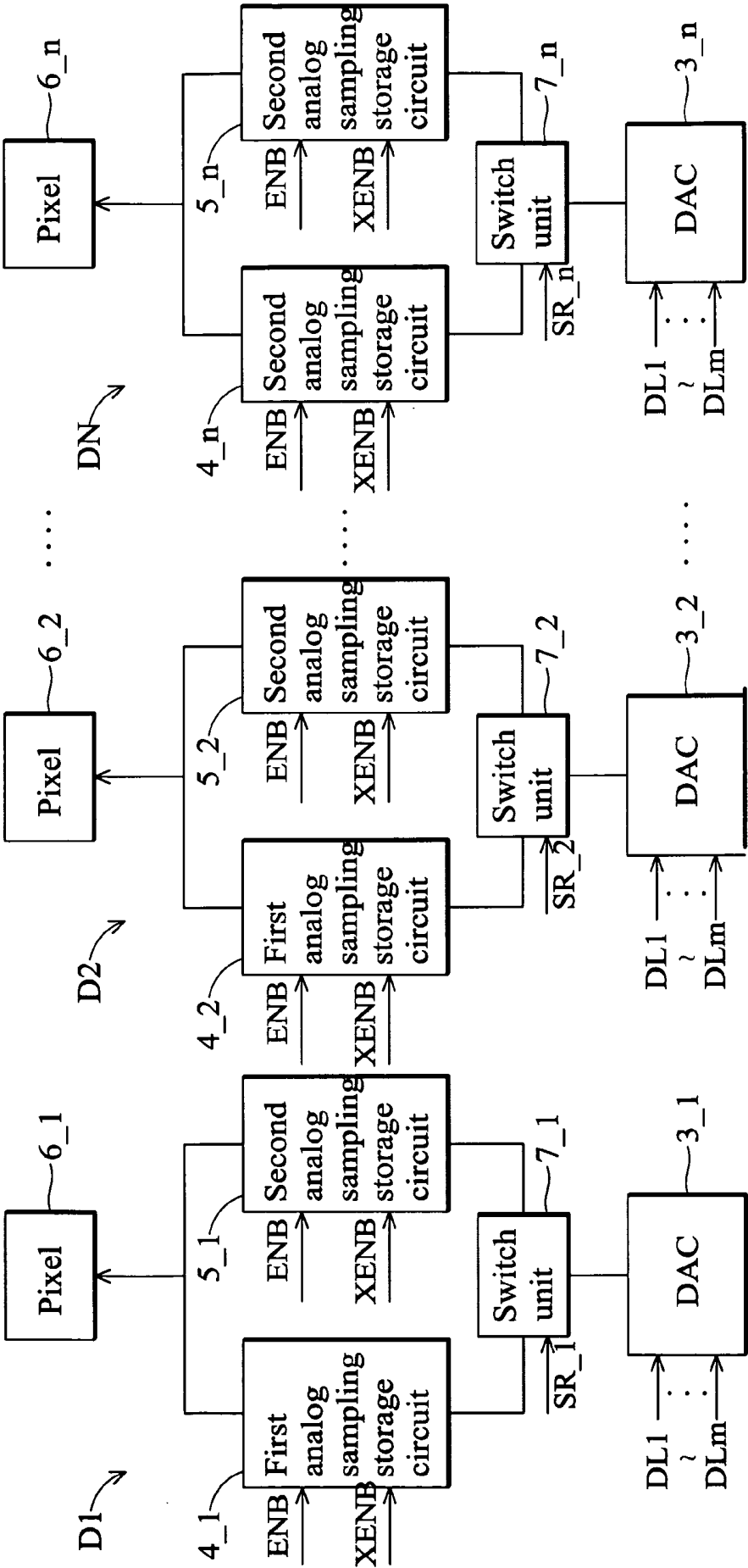


FIG. 3

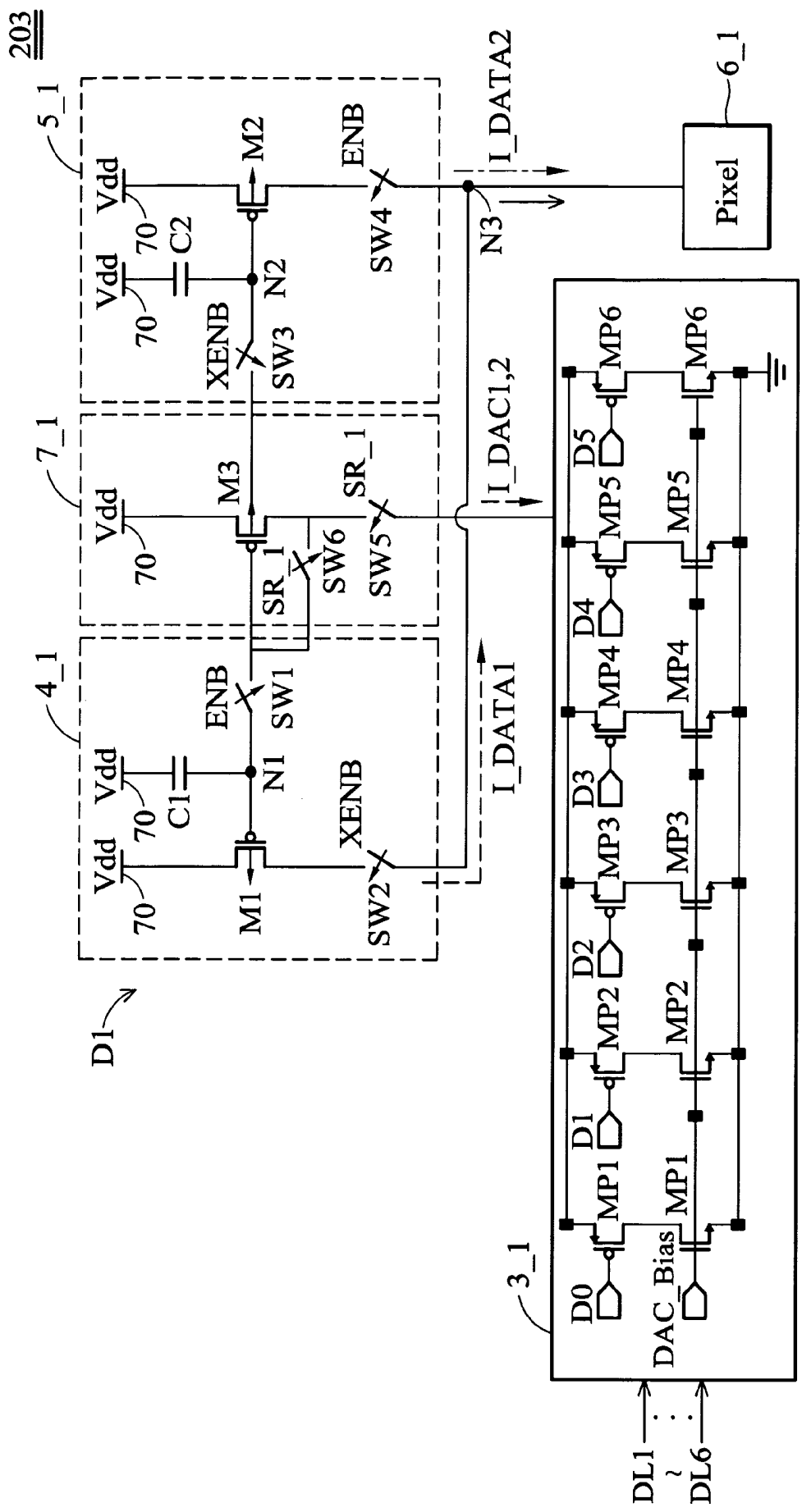


FIG. 4

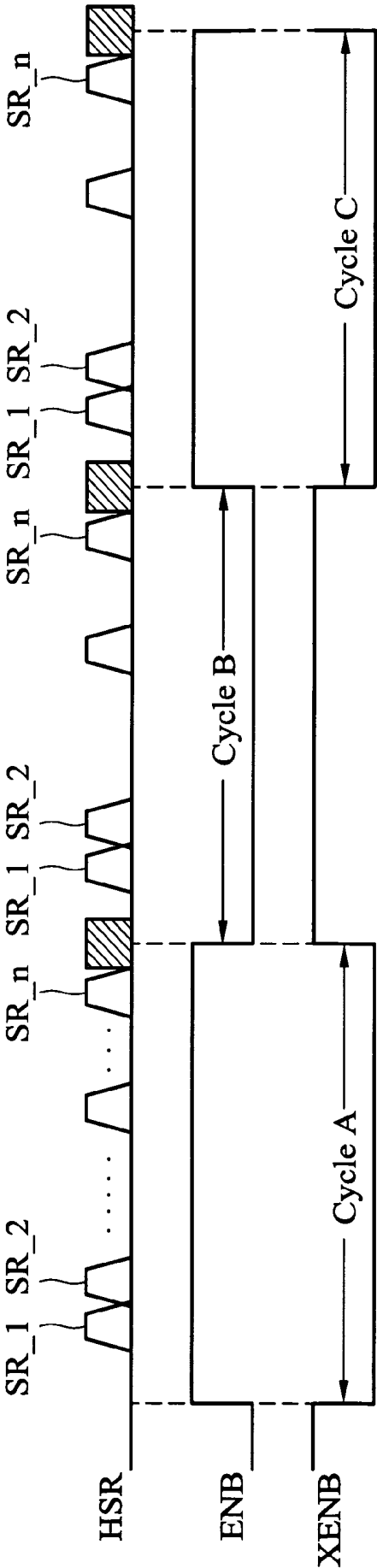


FIG. 5

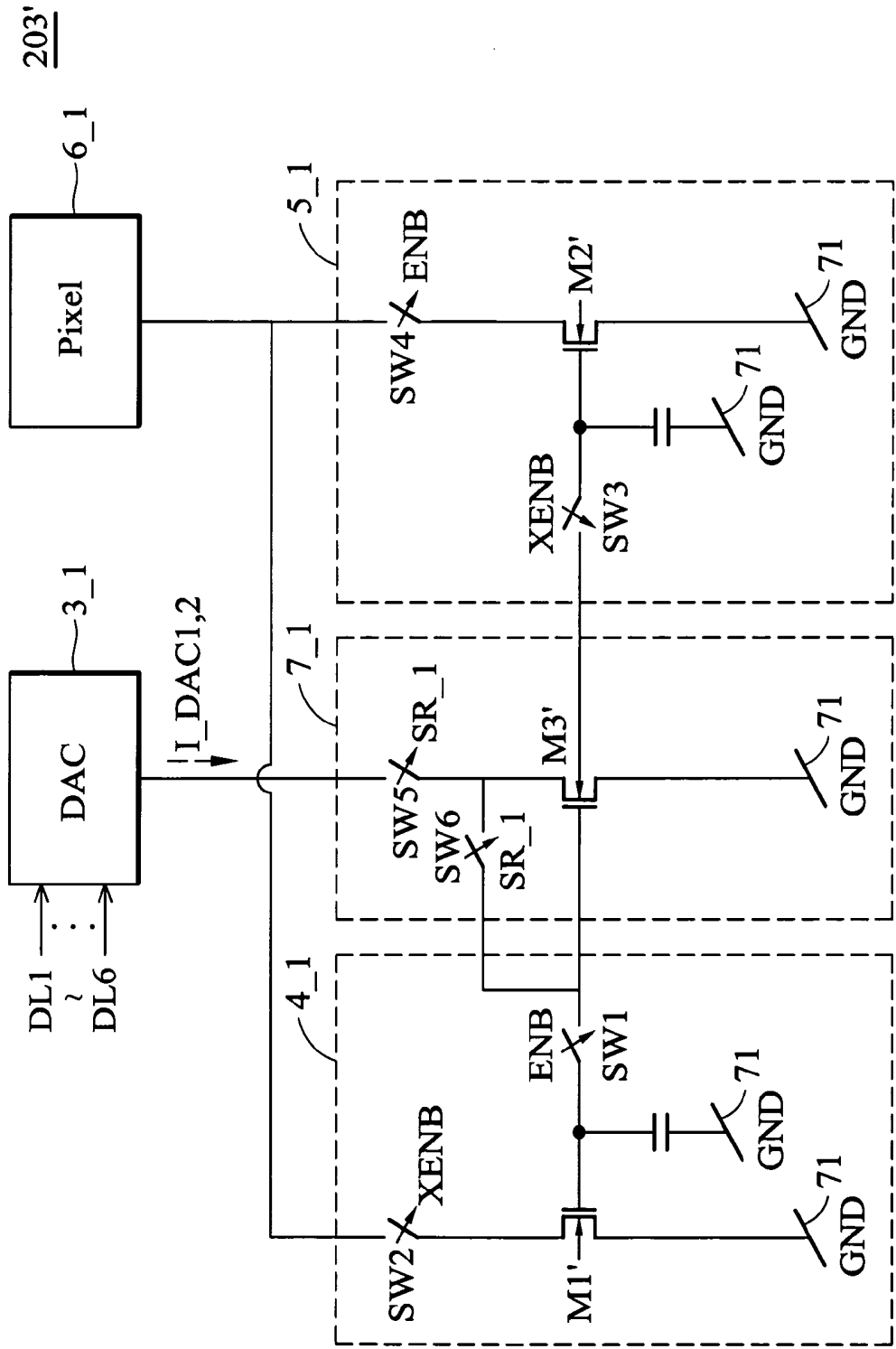


FIG. 6

DATA DRIVING CIRCUIT FOR ORGANIC LIGHT EMITTING DIODE DISPLAY

BACKGROUND

[0001] The invention relates to a data driving circuit and an organic light emitting diode display, and more particularly, to a data driving circuit without digital latches.

[0002] Digital data drivers of a conventional active organic light emitting display use a storage register, digital latch as a line buffer to store digital video data in a signal line cycle.

[0003] FIGS. 1A and 1B show conventional 6-bit digital data driving scheme 10. In the scheme 10, binary bits of digital video data are loaded sequentially during a horizontal scan cycle. First, through data lines R[5]~B[0] binary bits of digital video data are written to corresponding first latches 11, all controlled by a sampling signal applied by a shift register SR_n. Next, through data lines R[5]~B[0], binary bits of next digital video data are written to corresponding first latches 21, all controlled by a sampling signal applied by a shift register SR_{n+1}. Then, all bits of digital video data set are stored in the first latches 11 and 21 are written to the second latches 12 and 22 when the line buffer signal "LB" is asserted and transmitted to the digital-to-analog converters DAC-R_n, DAC-G_n, DAC-B_n at the same time.

[0004] The bit number of data increases as resolution goes higher, thus increasing the number of storage registers which occupy layout areas and increasing the number of digital-to-analog converters. In the conventional driving circuit layout, the bit number of data increases as resolution goes higher, and the number of storage registers and digital-to-analog converters are increased accordingly, making the layout more difficult, as the horizontal layout area of the digital data driving circuits is limited.

SUMMARY

[0005] It is an object of the present invention to provide a data driving circuit which comprises data lines transmitting first digital data in a first cycle and second digital data in a second cycle; a D/A converter (digital-to-analog converter) receiving the first digital data for transforming to corresponding first analog transformed data and receiving the second digital data for conversion to corresponding second analog transformed data; a switch unit coupled to the D/A converter and turned on by a sampling signal in the first cycle and the second cycle; a first analog sampling storage circuit coupled to the switch unit, controlled by a first signal for storing the first analog transformed data in the first cycle and controlled by a second signal for outputting first analog data corresponding to the first analog transformed data in the second cycle; and a second analog sampling storage circuit coupled to the switch unit, controlled by the second signal for storing the second analog transformed data in the second cycle and controlled by the first signal for outputting second analog data corresponding to the second analog transformed data in a third cycle.

[0006] The embodiment according to the present invention also provides an organic light emitting diode display, comprising a plurality of pixels arranged in an array form; a scan driving circuit turning on a row of the pixels in sequence; a data driving circuit comprising data lines trans-

mitting first digital data in a first cycle and second digital data in a second cycle, a D/A converter receiving the first digital data for transforming to corresponding first analog transformed data and receiving the second digital data for conversion to corresponding second analog transformed data, a switch unit coupled to the D/A converter and turned on by a sampling signal in the first cycle and the second cycle, a first analog sampling storage circuit coupled to the switch unit, controlled by a first signal for storing the first analog transforming data in the first cycle and controlled by a second signal for outputting first analog data corresponding to the first analog transformed data in the second cycle, and a second analog sampling storage circuit coupled to the switch unit, controlled by the second signal for storing the second analog transformed data in the second cycle and controlled by the first signal for outputting second analog data corresponding to the second analog transformed data in a third cycle.

[0007] A detailed description is given in the following with reference to the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] The invention can be more fully understood by reading the subsequent detailed description and examples with references made to the accompanying drawings, wherein:

[0009] FIG. 1A and FIG. 1B show conventional digital data driving circuits;

[0010] FIG. 2 illustrates an organic light emitting display;

[0011] FIG. 3 is a block circuit diagram of a data driving circuit of an embodiment of the invention;

[0012] FIG. 4 is a detailed circuit of a data driving circuit of an embodiment of the invention shown in FIG. 3;

[0013] FIG. 5 is a timing diagram of the data driving circuit of an embodiment of the invention; and

[0014] FIG. 6 is a circuit diagram of another embodiment of the invention.

DETAILED DESCRIPTION

[0015] FIG. 2 shows an organic light emitting diode display 200. As shown in FIG. 2, the organic light emitting diode display 200 comprises an active matrix array 201 substantially composed of a plurality of pixels, such as current driving pixels, a scan driving circuit 202 for turning on a row of pixels of the active matrix array 201 in sequence, and a data driving circuit 203 for outputting data to corresponding pixels.

[0016] FIG. 3 shows a block diagram of the data driving circuit 203 in FIG. 2. The data driving circuit 203 comprises a plurality of data driving units D1~DN, each comprising D/A converter 3_{1~3}_n, a switch unit 7_{1~7}_n, a first analog sampling storage circuit 4_{1~4}_n and a second analog sampling storage circuit 5_{1~5}_n.

[0017] The D/A converters 3_{1~3}_n are coupled to the data lines DL1~DL_m for transforming digital data to corresponding analog transforming data, such as current data, in a cycle. The switch units 7_{1~7}_n are coupled to corresponding D/A converters 3_{1~3}_n to be turned on by corresponding sampling signals SR₋SR_n in each cycle.

The first analog sampling storage circuits $4_1\sim 4_n$ are coupled to the switch units $7_1\sim 7_n$ for storing the analog transformed data when a first signal ENB is asserted in a cycle, or outputting analog data which corresponds to the analog transformed data stored in the last cycle to the corresponding pixels $6_1\sim 6_n$ when a second signal XENB is asserted. The second analog sampling storage circuits $5_1\sim 5_n$ are coupled to the switch units $7_1\sim 7_n$ for storing the analog transformed data when a second signal XENB is asserted in a cycle, or outputting analog data which corresponds to the analog transformed data stored in the last cycle to the corresponding pixels $6_1\sim 6_n$ when the first signal ENB is asserted.

[0018] FIG. 4 illustrates a detailed circuit of the data driving circuit D1 shown in FIG. 3. 6 bit data D0~D5 is transmitted to a 6-bit D/A converter 3_1. In the example, the D/A converter 3_1 is a typical 6-bit D/A converter.

[0019] Switch unit 7_1 comprises a transistor M3 as a current source, such as a PMOS transistor. The source of the transistor M3 is coupled to a voltage source 70, such as high voltage source Vdd. A gate of the transistor M3 is coupled to one end of the switch SW6 (the sixth switch). A drain of the transistor M3 is coupled to the switch SW5 and the other end of the switch SW6. The switch SW5 and the switch SW6 are turned on when a sampling signal SR_1 is asserted.

[0020] The first analog sampling storage circuit 4_1 comprises a storage capacitor C1, a transistor M1, a switch SW1 and a switch SW2. The storage capacitor C1 is set between the voltage source 70 and a node N1. The transistor M1 has a source coupled to the voltage source 70 and a gate coupled to the node N1. The switch SW1 (the first switch) is set between the storage capacitor C1 and the gate of the transistor M3 to be turned on or turned off according to the first signal ENB. The switch SW2 (the second switch) is set between a drain of the transistor M1 and a node N3 to be turned on or turned off according to the second signal XENB.

[0021] The second analog sampling storage circuit 5_1 comprises a storage capacitor C2, a transistor M2, a switch SW3, and a switch SW4. The storage capacitor C2 is set between a voltage source 70 and a node N2. The transistor M2 has a source coupled to the voltage source 70, and a gate coupled to the node N2. A switch SW3 (the third switch) set between the storage capacitor C2 and the gate of the transistor M3 to be turned on or turned off according to the second signal XENB. Switch SW4 (the fourth switch) set between a drain of the transistor M2 and the node N3 to be turned on or turned off according to the first signal ENB.

[0022] FIG. 5 is a timing diagram of the data driving circuit 203 in FIG. 4. First, in cycle A (the first cycle), digital data D0~D5 (first digital data) are transmitted to the D/A converter 3_1 through corresponding data lines DL1~DL6 for conversion to corresponding analog data I_DAC1 (first analog transforming data), such as current data. At the same time, a sampling signal SR_1 is applied to turn on switches SW5 and SW6. A first signal ENB is asserted to turn on switch SW1. Analog data I_DAC1 is written to the storage capacitor C1 through switch SW5, SW6 and SW1.

[0023] In cycle B (the second cycle), the first signal ENB is desasserted to turn off switch SW1. The second signal XENB is asserted to turn on switches SW2. The analog data

I_DAC1 of the storage capacitor C1 is sent to the gate of the transistor M1 for outputting a corresponding analog data I_DATA1 to pixel 6_1. At the same time, another digital data D0~D5 (second digital data) are written into D/A converter 3_1 for conversion to corresponding analog data I_DAC2 (second analog transforming data), such as current data. When the switch SW5 and switch SW6 are turned on by the sampling signal SR_1, and switch SW3 is turned on by the second signal XENB. The analog data I_DAC2 (second analog transforming data) is written to the storage capacitor C2 through switches SW5 SW6 and SW3.

[0024] In cycle C (the third cycle), the second signal XENB is desasserted to turn off switch SW3, and the first signal ENB is asserted to turn on switch SW4. The analog data I_DAC2 of the storage capacitor C2 is sent to the gate of the transistor M2 for outputting a corresponding analog data I_DATA2 to pixel 6_1.

[0025] FIG. 6 shows another embodiment of the data driving circuit 203' of the invention. The difference between the data driving circuit 203' and the data driving circuit 203 shown in FIG. 4 is that the transistors M1'~M3' are NMOS transistors, and the voltage source is a low voltage source Vss.

[0026] A driving method of embodiments of the invention is also disclosed. Through data lines, first and second digital data are received by a D/A converter in first and second cycle respectively, for conversion to first and second analog transformed data. The first analog transformed data is stored to a first analog sampling storage circuit in the first cycle. In the second cycle, first analog data corresponding to the first analog transformed data is output to drive to a pixel while the second analog transformed data is stored to a second analog sampling storage circuit. In a third cycle adjacent to the second cycle, second analog data corresponding to the second analog transformed data is output to drive to the pixel.

[0027] While the invention has been described by way of example and in terms of preferred embodiment, it is to be understood that the invention is not limited thereto. On the contrary, it is intended to cover various modifications and similar arrangements as would be apparent to those skilled in the art. Therefore, the scope of the appended claims should be accorded the broadest interpretation to encompass all such modifications and similar arrangements.

What is claimed is:

1. A data driving circuit comprising:

a D/A converter for receiving first digital data from data lines in a first cycle to convert to first analog transformed data, and receiving second digital data from the data lines in a second cycle to convert to second analog transformed data;

a switch unit coupled to the D/A converter; a first analog sampling storage circuit, coupled to the switch unit, for storing the first analog transformed data in the first cycle, and outputting first analog data corresponding to the first analog transformed data in the second cycle; and

a second analog sampling storage circuit, coupled to the switch unit, for storing the second analog transformed

data in the second cycle, and outputting second analog data corresponding to the second analog transformed data in a third cycle.

2. The data driving circuit as claimed in claim 1, wherein the first analog sampling storage circuit comprises:

- a first storage capacitor coupled to a voltage source and a first node;
- a first transistor coupled to the voltage source and a pixel, a gate of the first transistor being coupled to the first node;
- a first switch coupled to the first storage capacitor and the switch unit; and
- a second switch coupled to the first transistor and the pixel.

3. The data driving circuit as claimed in claim 2, wherein the second analog sampling storage circuit comprising:

- a second storage capacitor coupled to the voltage source and a second node;
- a second transistor coupled to the voltage source and the pixel, a gate of the second transistor being coupled to the second node;
- a third switch coupled to the second storage capacitor and the switch unit; and
- a fourth switch coupled to the second transistor and the pixel.

4. The data driving circuit as claimed in claim 3, wherein the switch unit comprises:

- a third transistor, having a first end coupled to the voltage source, a second end coupled to the first switch and the third switch, and a third end coupled to the D/A converter through a fifth switch and coupled to the first switch and the third switch through a sixth switch.

5. The data driving circuit as claimed in claim 4, wherein the first through the sixth switches are transistors or transmission gates.

6. An organic light emitting diode display, comprising:

- a plurality of pixels arranged in an array form;
- a scan driving circuit for turning on a row of the pixels in sequence; and

A data driving circuit comprising:

- a D/A converter for receiving first digital data from data lines in a first cycle to convert to first analog transformed data, and receiving second digital data from the data lines in a second cycle to convert to second analog transformed data;
- a switch unit coupled to the D/A converter;
- a first analog sampling storage circuit, coupled to the switch unit, for storing the first analog transformed data in the first cycle, and outputting first analog data corresponding to the first analog transformed data to a corresponding pixel in the second cycle; and
- a second analog sampling storage circuit, coupled to the switch unit, for storing the second analog transformed data in the second cycle, and outputting

second analog data corresponding to the second analog transformed data to the corresponding pixel in a third cycle.

7. The organic light emitting diode display as claimed in claim 6, wherein the first analog sampling storage circuit comprises:

- a first storage capacitor coupled to a voltage source and a first node;
- a first transistor coupled to the voltage source and the corresponding pixel, a gate of the first transistor being coupled to the first node;
- a first switch coupled to the first storage capacitor and the switch unit; and
- a second switch coupled to the first transistor and the corresponding pixel.

8. The organic light emitting diode display as claimed in claim 7, wherein the second analog sampling storage circuit comprises:

- a second storage capacitor coupled to the voltage source and a second node;
- a second transistor coupled to the voltage source and the corresponding pixel, a gate of the second transistor being coupled to the second node;
- a third switch coupled to the second storage capacitor and the switch unit; and
- a fourth switch coupled to the second transistor and the corresponding pixel.

9. The organic light emitting diode display as claimed in claim 8, wherein the switch unit comprises:

- a third transistor having a first end coupled to the voltage source, a second end coupled to the first switch and the third switch, and a third end coupled to the D/A converter through a fifth switch and coupled to the first switch and the third switch through a sixth switch.

10. The organic light emitting diode display as claimed in claim 9, wherein the first through the sixth switches are transistors or transmission gates.

11. A driving method comprising the steps of:

- converting first digital data to first analog transformed data in a first cycle;
- converting second digital data to second analog transformed data in a second cycle;
- storing the first analog transformed data to a first analog sampling storage circuit in the first cycle;
- outputting first analog data corresponding to the first analog transformed data to a pixel in the second cycle;
- storing the second analog transformed data to a second analog sampling storage circuit in the second cycle; and
- outputting second analog data corresponding to the second analog transformed data to the pixel in a third cycle.

12. The driving method as claimed in claim 11, wherein the step of storing the first analog transformed data comprises:

- providing a first signal to turn on a first switch in the first cycle; and

storing the first analog transformed data to a first storage capacitor in the first cycle.

13. The driving method as claimed in claim 11, wherein the step of outputting the first analog data comprises:

providing a first signal to turn off a first switch in the second cycle;

providing a second signal to turn on a second switch in the second cycle; and

outputting the first analog data from a first storage capacitor to the pixel through a first transistor in the second cycle.

14. The driving method as claimed in claim 11, wherein the step of storing the second analog transformed data comprises:

providing a first signal to turn on a first switch in the second cycle; and

storing the second analog transformed data to a first storage capacitor in the second cycle.

15. The driving method as claimed in claim 14, wherein the step of outputting the second analog data comprises:

providing the first signal to turn off the first switch in the third cycle;

providing a second signal to turn on a second switch in the third cycle; and

outputting the second analog data from the first storage capacitor to the pixel through a first transistor in the third cycle.

16. The driving method as claimed in claim 11, further comprising a step of providing a sampling signal to turn on a fifth switch and a sixth switch.

* * * * *

专利名称(译)	用于有机发光二极管显示器的数据驱动电路		
公开(公告)号	US20050270206A1	公开(公告)日	2005-12-08
申请号	US11/125992	申请日	2005-05-10
[标]申请(专利权)人(译)	友达光电股份有限公司		
申请(专利权)人(译)	友达光电.		
当前申请(专利权)人(译)	友达光电.		
[标]发明人	TSENG JUNG CHUN YEH SHIN HUNG SUN WEIN TOWN		
发明人	TSENG, JUNG-CHUN YEH, SHIN-HUNG SUN, WEIN-TOWN		
IPC分类号	G09G3/20 G09G3/32 H03M1/66		
CPC分类号	G09G3/2025 G09G2310/027 G09G3/3275 G09G3/2081		
优先权	093114377 2004-05-21 TW		
其他公开文献	US7525524		
外部链接	Espacenet USPTO		

摘要(译)

一种数据驱动电路和有机发光二极管显示器，包括D/A转换器，开关单元，第一模拟采样存储电路和第二模拟采样存储电路。第一模拟采样存储电路由第一信号控制，第一信号用于在第一周期中存储相应第一模拟变换数据，并由第二信号控制，用于输出与第二周期中的第一模拟变换数据相对应第一模拟数据。第二模拟采样存储电路由第二信号控制，用于在第二周期中存储第二模拟变换数据，并由第一信号控制，用于在第三周期中输出对应于第二模拟变换数据的第二模拟数据。

